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09/975,066	10/12/2001	Toshiharu Seko	925-214	9995

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EXAMINER

THAI, LUAN C

ART UNIT

PAPER NUMBER

2827

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/975,066

Applicant(s)

SEKO, TOSHIHARU

Examiner

Luan Thai

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 October 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4. 6) ☐ Other: ____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS), filed on 10/26/01, has been considered by the examiner.

Priority

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in *Japan* on 10/13/2000.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sozansky et al. (5,953,814).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 9, Sozansky et al disclose (see specifically figures 1-2) a tape 10 for chip on film on which a semiconductor element 12 is mounted and resin 20 is applied for sealing the semiconductor element, the tape for chip on film comprising: an insulating tape 10; a plurality of wiring patterns 16 formed on the insulating tape; a solder resist 22 partially covering the wiring patterns 16 by

application to have an opening 24 (see figure 2). Sozansky et al disclose (as applicant claimed) that an opening edge of the solder resist opposed to a corner of a region for the semiconductor element to be mounted is located in a vicinity of the corner, and a shape of the opening edge of the solder resist in the vicinity of the corner is made along a shape of the corner.

Although Sozansky et al do not explicitly state that the shape of the opening edge of the solder resist along the shape of the corner would control the flow of resin from the corner to the space between a surface of the semiconductor element and the insulating tape, Applicant's claimed structure in claim 9 does not distinguish over the Sozansky et al references and it has been held that a recitation (e.g., to control the flow of the resin from the corner to the space between a surface of the semiconductor element and the insulating tape) with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

5. Claims 10-11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sozansky et al. (5,953,814) in view of Hayakawa et al. (4,280,132).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 10-11, the proposed device of Sozansky et al discloses all the limitations of the claimed invention, including the inner leads 26, as

detailed above except for the inner leads have a large width section wider than an electric connection section of the inner leads connected to the semiconductor element.

An inner lead having a large width section wider than an electric connection section of the inner lead connected to the semiconductor element and positioned at the corner of a region for the semiconductor element to be mounted, however, is conventional in the art, as disclosed by Hayakawa et al (see figure 3). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the inner lead having a large width section wider than an electric connection section of the inner lead connected to the semiconductor element and positioned at the corner of a region for the semiconductor element to be mounted since such inner lead structure and its position in a device package are conventional in the art, as disclosed by Hayakawa et al.

Furthermore, although the proposed structure device of Sozansky et al and Hayakawa et al does not explicitly state that the large width section of the inner lead positioned at the corner of the region would control the flow of the resin from the corner to the space between a surface of the semiconductor element and the insulating tape, Applicant's claimed structure in claims 10-11 does not distinguish over the proposed structure device of Sozansky et al and Sato and it has been held that a recitation (e.g., to control the flow of resin from the corner to the space between a surface of the semiconductor element and the

insulating tape) with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

The further citations of claim 14 would have been obvious for the similar reasons set forth in the discussion of claim 9 above.

6. Claims 1-2, 5-8, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sozansky et al. (5,953,814) in view of Sato (6,287,895).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1-2, 5-8, 15 and 18, Sozansky et al (see specifically figures 1-2) a tape for chip on film on which a semiconductor element 12 is mounted and resin 20 is applied for sealing the semiconductor element, the tape for chip on film comprising: an insulating tape 10; a plurality of wiring patterns 16 formed on the insulating tape; a solder resist 22 partially covering the wiring patterns 16 by application to have an opening 24 (see figure 2); a dummy pattern 28 formed on the insulating tape and inherently having a same thickness with the wiring pattern 16 (Col. 6, lines 42+); a sealing resin 20 sealing the semiconductor and a surface of the insulating tape 10. Sozansky et al do not explicitly teach that the dummy pattern 28 is provided at a corner of the region for the semiconductor element to be mounted to control flow of the resin from the corner to a space

between a surface of the semiconductor element and the insulating tape during resin sealing.

Dummy patterns provided at corners of the region for the semiconductor element to be mounted, however, are conventional in the art as disclosed by Sato (see figures 1A-1B). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dummy patterns 28 at corners of the region for the semiconductor element to be mounted since such position of the dummy patterns on the insulating board is conventional in the art, as disclosed by Sato. Further, although the proposed structure device of Sozansky et al and Sato does not explicitly state that the dummy patterns at the corners would control the flow of the resin from the corner to the space between a surface of the semiconductor element and the insulating tape, Applicant's claimed structure in claims 1-2, 5-8, 15 and 18 does not distinguish over the proposed structure device of Sozansky et al and Sato and it has been held that a recitation (e.g., to control the flow of resin from the corner to the space between a surface of the semiconductor element and the insulating tape) with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex Parte Masham*, 2 USPQ F.2d 1647 (1987).

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7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sozansky et al. (5,953,814) in view of Sato (6,287,895) and further in view of Terashima (6,157,085).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 4, the proposed device of Sozansky et al. and Sato discloses all the limitations of the claimed invention as detailed above except for the dummy pattern provided inside the opening of the solder resist and extended from outside to inside the corner.

The dummy pattern provided inside the opening of the solder resist and extended from outside to inside the corner, however, is conventional in the art as disclosed by Hayakawa et al (see pattern 3' in figure 1 to be considered as the claimed dummy pattern). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dummy pattern provided inside the opening of the solder resist and extended from outside to inside the corner, since such dummy pattern structure is conventional in the art as disclosed by Terashima.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sozansky et al. (5,953,814) in view of Hayakawa et al. (4,280,132) and further in view of Terashima (6,157,085).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 12, the proposed device of Sozansky et al and Hayakawa et al. discloses all the limitations of the claimed invention as detailed above except for the large width section of the inner leads disposed from outside or inside a border line of the region for the semiconductor element to be mounted to inside a region for the solder resist to be applied.

The large width section of the inner leads disposed from outside a boarder line of the region for the semiconductor element to be mounted to inside a region for the solder resist to be applied, however, is conventional in the art, as taught by Terashima (see figures 5-6-7-8). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the inner leads having the large width sections disposed from outside a boarder line of the region for the semiconductor element to be mounted to inside a region for the solder resist to be applied, since such structure of the inner leads is conventional in the art as taught by Terashima.

9. Claims 13 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sozansky et al. (5,953,814) in view of Hayakawa et al. (4,280,132) and further in view of Sato (6,287,895).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 13 and 16-17, the proposed device of Sozansky et al and Hayakawa et al discloses all the limitations of the claimed invention as detailed above except for dummy pattern 28 is provided at a corner of the region for the semiconductor element to be mounted to control flow of the resin from the corner to a space between a surface of the semiconductor element and the insulating tape during resin sealing.

Dummy patterns provided at corners of the region for the semiconductor element to be mounted, however, are conventional in the art as disclosed by Sato (see figures 1A-1B). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the dummy patterns 28 at corners of the region for the semiconductor element to be mounted since such position of the dummy patterns on the insulating board is conventional in the art, as disclosed by Sato. Furthermore, although the proposed structure device discussed above does not disclose that the dummy patterns at the corners would control the flow of the resin from the corner to the space between a surface of the semiconductor element and the insulating tape, Applicant's claimed structure in claims 13 and 16-17 does not distinguish over the proposed structure device as discussed above and it has been held that a recitation (e.g., to control the flow of resin from the corner to the space between a surface of the semiconductor element and the insulating tape) with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed

apparatus from a prior art apparatus satisfying the claimed structural limitations.

Ex Parte Masham, 2 USPQ F.2d 1647 (1987).

10. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sozansky et al. (5,953,814) in view of Sato (6,287,895) and further in view of Hayakawa et al. (4,280,132).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claim 3, the proposed device of Sozansky et al. and Sato discloses all the limitations of the claimed invention as detailed above except for a shape of the dummy pattern being formed along a shape of the corner.

A shape of the dummy pattern being formed along a shape of the corner of the region for the semiconductor element to be mounted, however, is conventional in the art as disclosed by Hayakawa et al (see dummy pattern 20 in figure 1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a dummy pattern having a shape along a shape of the corner of the region for the semiconductor element to be mounted, since such dummy pattern structure is conventional in the art as disclosed by Hayakawa et al.

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11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is (703) 308-1211. The examiner can normally be reached on 7:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on (703) 305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Luan Thai
October 2, 2002

Albert W. Paladini 10-18-02
ALBERT W. PALADINI
PRIMARY EXAMINER